

The diagram shows a 10-transistor CMOS logic circuit with four stages labeled 1, 2, 3, and 4. Stage 1 is a PMOS-only buffer where the input IN is connected to the gates of TR9 and TR10, and the output OUT is taken from the common drain connection. Stage 2 is a CMOS inverter with TR1 (PMOS) and TR2 (NMOS). Stage 3 is a CMOS inverter with TR5 (PMOS) and TR6 (NMOS). Stage 4 is a CMOS inverter with TR7 (PMOS) and TR8 (NMOS). The output of stage 4 is connected to the input of stage 1. Clock signals CK and CKX are connected to the gates of TR2, TR6, and TR8. All PMOS transistors (TR1, TR5, TR9) have their sources connected to Vcc, and all NMOS transistors (TR2, TR3, TR4, TR6, TR7, TR8, TR10) have their sources connected to ground.

(A) IN

(B) CK CKX

(C)

(D) OUT

FIG. 3

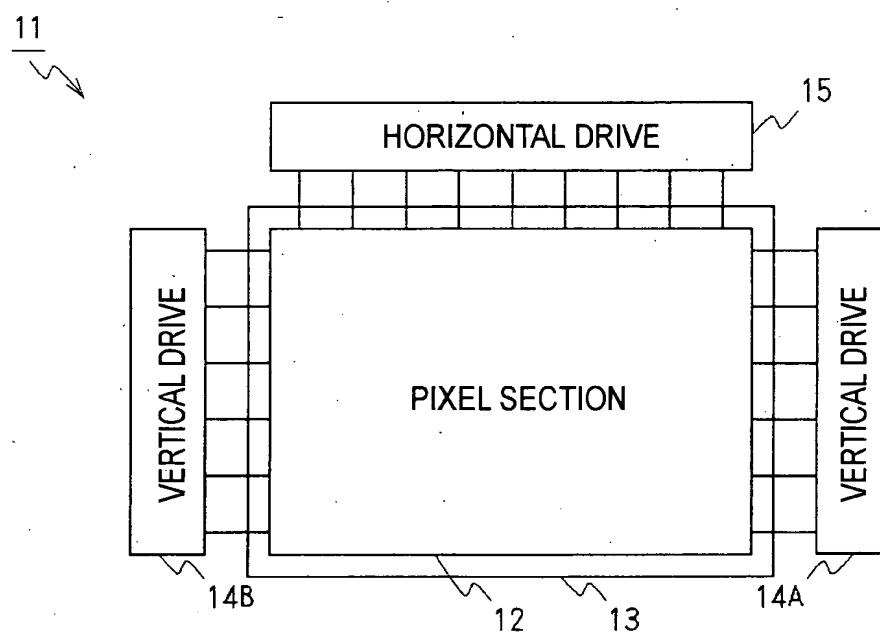
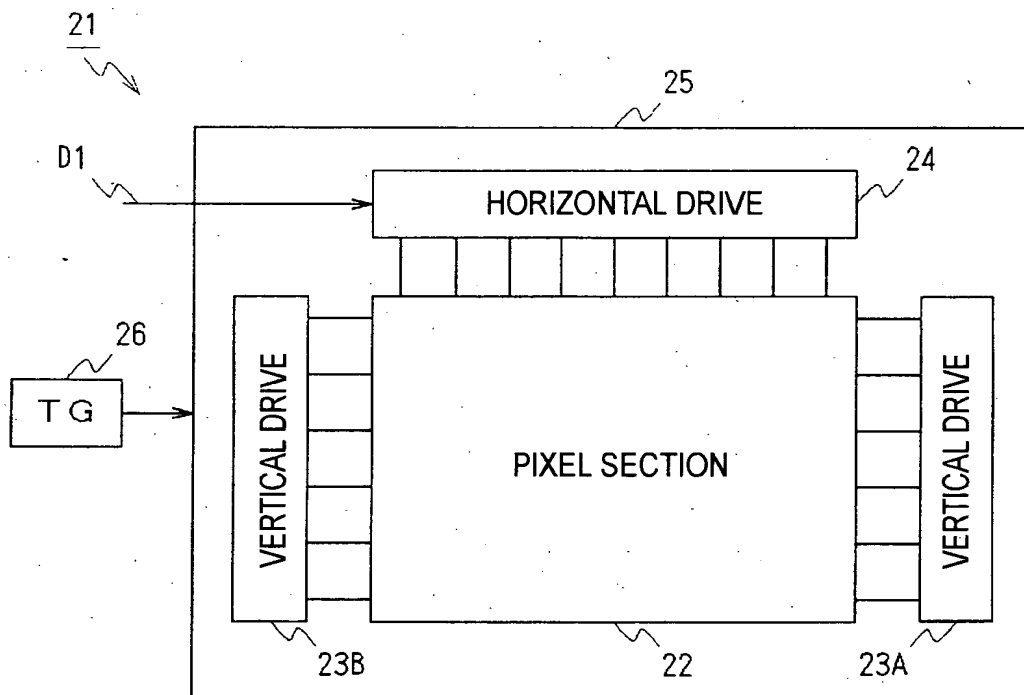
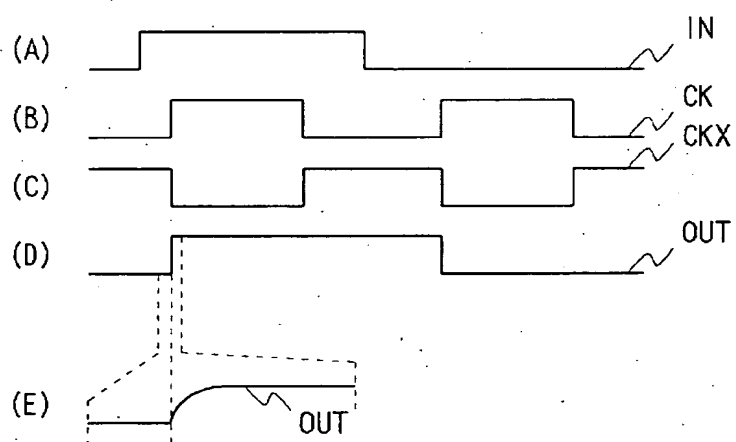


FIG. 4



[illegible]

FIG. 6



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FIG. 7

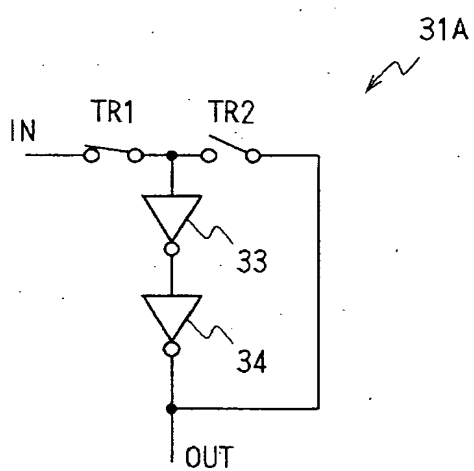
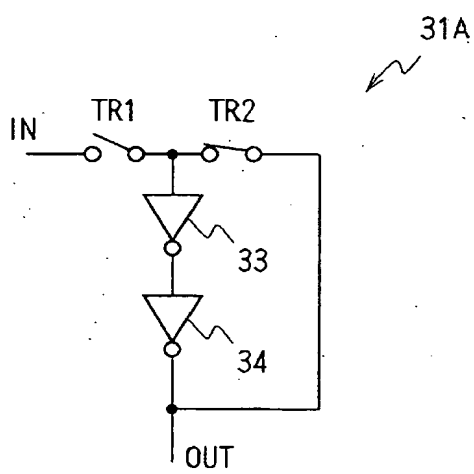


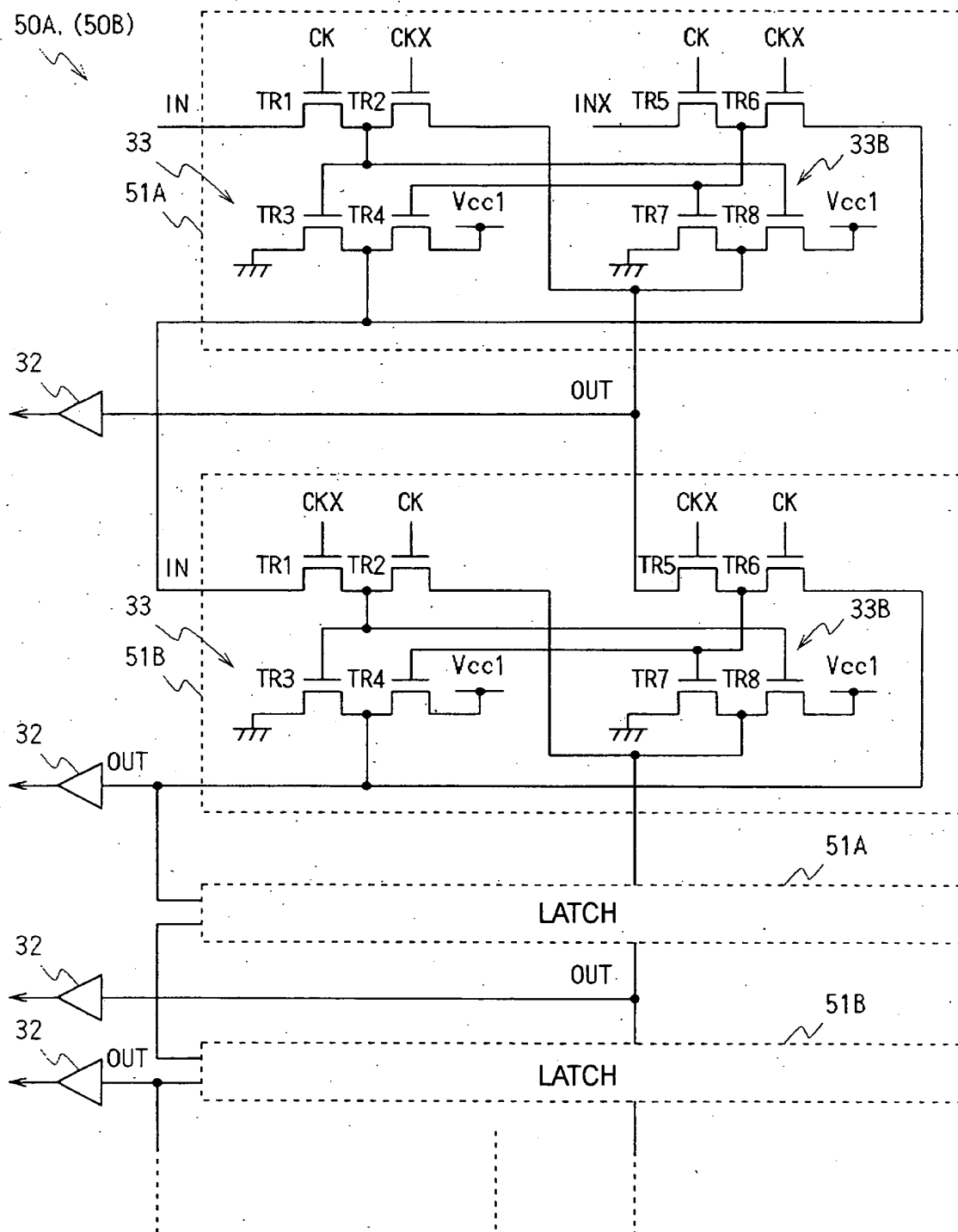
FIG. 8



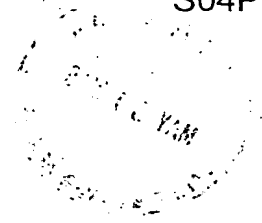


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FIG. 10







## DESCRIPTION OF REFERENCE CHARACTER

1, 31A, 31B, 41A, 41B, 51A, 51B ..... LATCH CIRCUIT, 2, 3 .....  
CLOCKED INVERTER CIRCUIT, 4, 33, 33A, 33B, 34, 34A .....  
INVERTER CIRCUIT, 11, 21 ..... FLAT DISPLAY APPARATUS, 12,  
22 ..... PIXEL SECTION, 13, 25 ..... GLASS SUBSTRATE, 14A,  
14B, 23A, 23B, 40A, 40B, 50A, 50B ..... VERTICAL DRIVE  
CIRCUIT, 15, 24 ..... HORIZONTAL DRIVE CIRCUIT, 26 .....  
TIMING GENERATOR, 32 ..... BUFFER CIRCUIT, TR1 - TR12  
..... TRANSISTOR